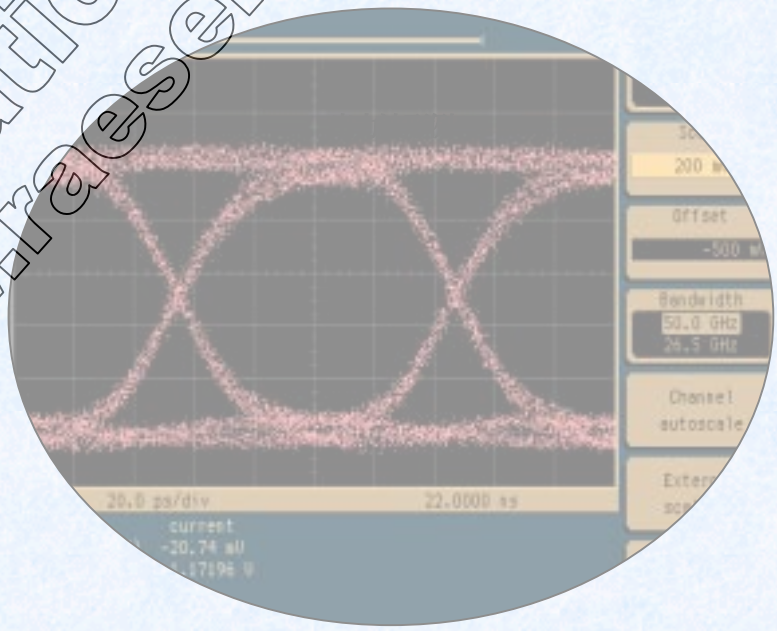
11G BERT MODULE

AP9943

- Optical Transmission Component Test up to 2.5G bit/s～10.66G bit/s
- Mass-production test of the transmission module based on SONET/SDH
- It is possible to use as super-high speed PRBS pattern signal generation source of 40Gbit/s



Simple BERT for mass-production test of transmission component

AP9943 11G BERT MODULE is the simple measuring instrument for an electric interface test of the optical fiber transmission component and a MUX/DEMUX circuit used by the DWDM Transmission system. Connecting AP9943 to the electric input and output interface part of an optical fiber transmission component, it is possible to measure the bit error and the durability of CDR (clock detection recovery) as a signal generation source and a receiving part. Moreover, carrying out two or more modules of AP9943, evaluation time can be shorten and MUX/DEMUX circuit of super-high-speed 40G bit/s can be evaluated.

AP9943 is the system, which is developed as a module of VXI bus main flame for measuring instrument industry standard, can correspond to various measurement needs together with other VXI modules.

The features and functions

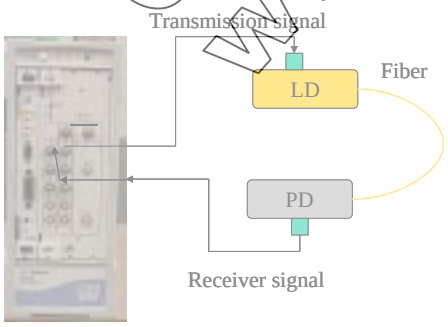
- **Multi bit rate correspondence**

  2.48G bit/s, 2.66G bit/s, 9.95G bit/s, 10.66G bit/s

- **Abundant BER test patterns**
  - PRBS Pattern: 2^7-1, 2^{15}-1, 2^{23}-1, 2^{31}-1
  - Program Pattern: 8192 byte length
  - Simple frame pattern (SDH-like frame generation and reception)
  - CDR test pattern (The pattern of ITU-T G.958 conformity)
- **The graphical user interface of easy operation**
- **Capable to use signal generation source and detector for MUX/DEMUX test by 10G bit/s x 4ch.(40G bit/s)**

Measurement image figures

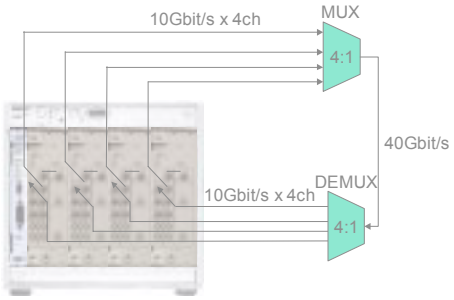
10G Optical transmission module test image



Agilent made E8408A Example mounted on VXI main frame

MUX/DEMUX test image

MUX/DEMUX test by 10G x 4ch.



Agilent made E8403A Example mounted on VXI main frame

Applications

Transmitting part test

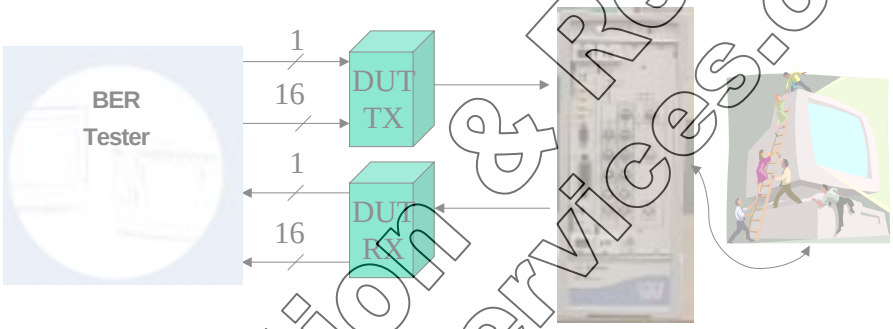
- Operation Bit Rate: 2.488/ 2.66/ 9.95/ 10.66G bit/s
  Frequency offset is provided with ±50 ppm variation.
- Pattern dependency: Generate PRBS pattern, a program pattern, and SDH frame pattern and check if there is no pattern dependency.
- Add some errors onto the test pattern to check the test object.

Receiving part test

- Operation Bit Rate: Confirm that any error does not occur with 2.48/ 2.66/ 9.95/ 10.66G bit/s
- Pattern dependency: Confirm pattern dependency with PRBS pattern、Program pattern、SDH Frame pattern. Input CID (0/1 continuation pattern) pattern, and measure the CDR durability.
- Error rate curve measurement: Attenuate the optical incoming signal level and measure the error rate curve.

Test for the module, which has MUX/DEMUX Interface

MUX/DEMUX interface test, which has adopted Low-Voltage Differential Signal (LVDS), can test together with other measuring instruments.

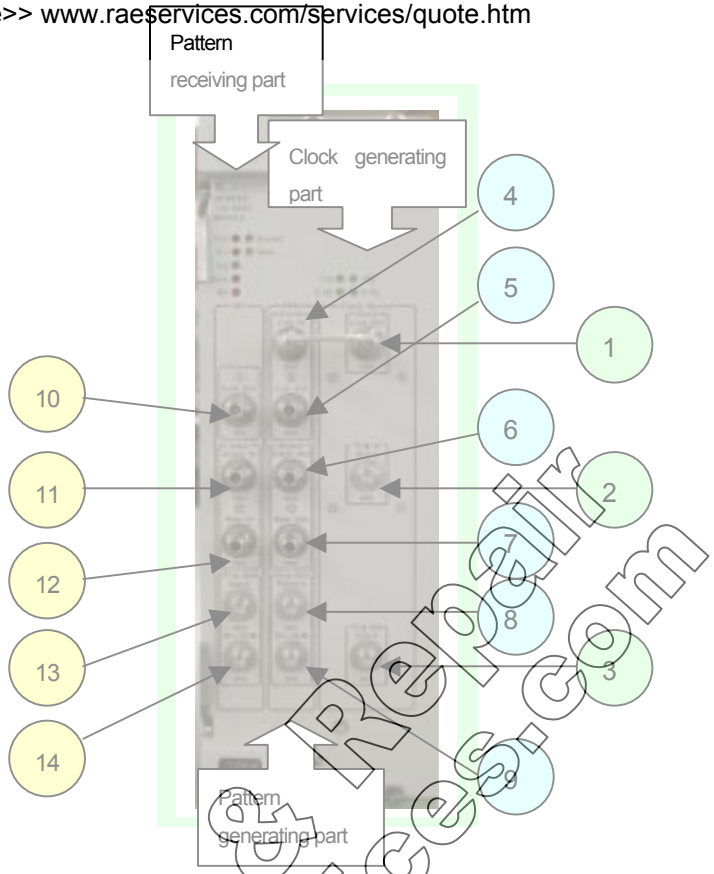


Configuration of Measuring Instrument

Model name	Item name	Outline	Note
AP9943	11G BERT MODULE	Compatible with 2.5Gbit/s ~ 10.66Gbit/s Electric interface BER measurement VXI C size 3 slot width	Instruction manual: 1pc Software (CD-ROM): 1pc Connection cable: 1pc 50 Ω Terminator: 4pcs
The recommendation products for AP9943 (in order to measure, the following recommendation articles are needed for AP9943.)			
VXI main frame		VXI mainframe to install a VXI module	
VXI command module		Command module to communicate with PC controller.	
PC (Personal Computer)		PC to control the AP9943.	Windows95/98/NT CPU Speed: Pentium II 200MHz or higher HD volume: Need more than 20MB RAM volume: Recommend more than 64MB
GPIB Interface card		This interface card is installed into PC.	Confirmed the operation with NI and Agilent product. VISA driver and GPIB cable are needed.

Related model: AP9942B SDH/SONET Analyzer

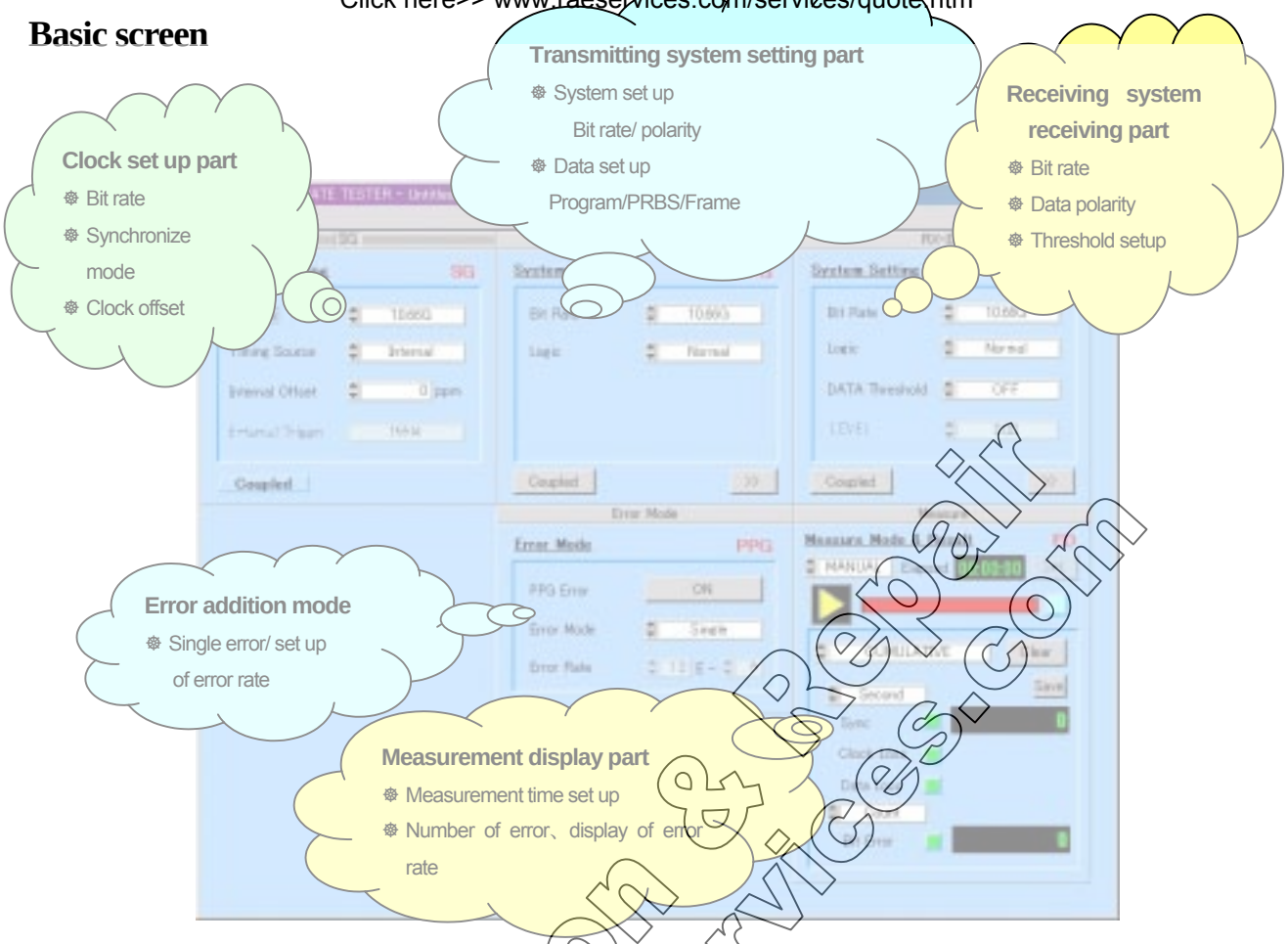
Front View of Module

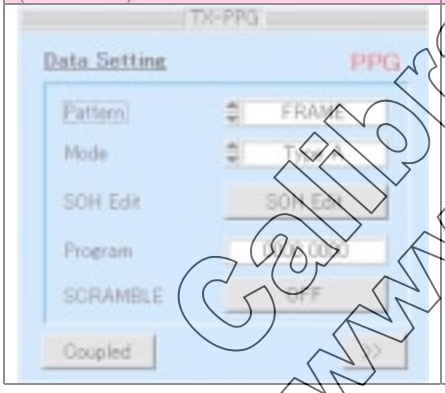
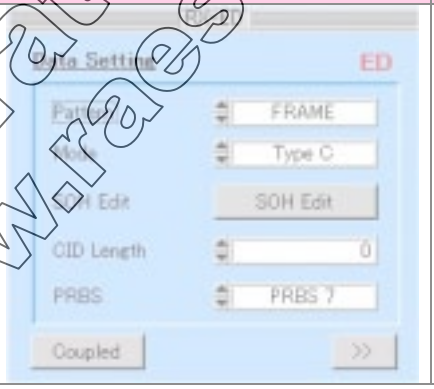
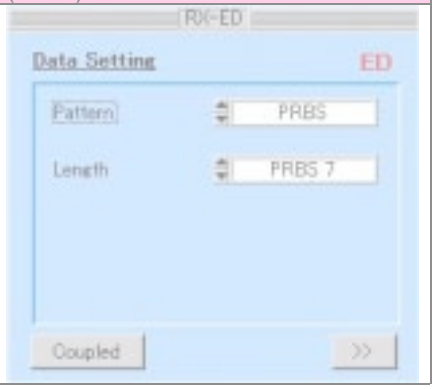


No	Name of connector	Remarks
1	Clock Line Out	Provide clock to pattern generating part ● Clock: 10.6642GHz, 9.95328GHz, 2.66606GHz, 2.48832GHz ● Output level: 1Vpp (Nominal)
2	Trig In Slave	External clock signal input terminal. Operate with external synchronization clock signal subordinately. Input frequency: 155.52MHz, 166.63MHz Minimum operation signal level: more than 0.6Vpp.
3	Trig Out Clock	Clock out trigger output. The trigger signals for a synchronization, such as eye pattern observation 155.52MHz: When clock output is 9.95GHz/ 2.488GHz 166.63GHz: When clock output is 10.66GHz/ 2.66GHz
4	Clock Line In	Standard clock input for pattern generation ● Clock: 10.6642GHz, 9.95328GHz, 2.66606GHz, 2.48832GHz ● Signal level: More than 0.7Vpp.
5	Clock Line Out	Clock signal output, which branches line clock incoming signal. Use for cascade connection of clock.
6	Output Clock Out	Clock signal output terminal. Provide clock for test object.
7	Output Data Out	Data signal output terminal. Provide data for test object.
8	Trig Out Pattern	Periodic trigger signal output which synchronized with the data output
9	Trig Out Error	Output pulse at the time when error is added.
10	ED Clock Line Out	Branches the signal inputted into the Clock In and output clock.
11	Input Clock In	Clock input terminal for receiving the clock signal outputted from test object.
12	Input Data In	Data input terminal for receiving the data signal outputted from test object.
13	Trig Out Slave	Output trigger signal of the divided signal of frequency inputted into clock input terminal.
14	Trig Out Err	Output error trigger signal when the error occurs with the data pattern inputted into data input terminal.

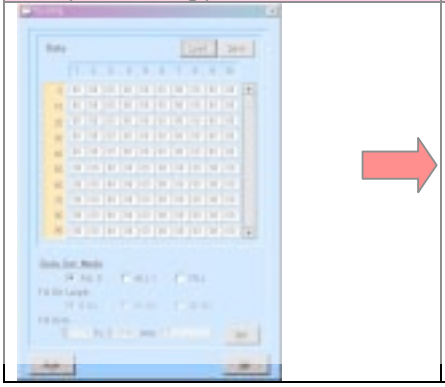
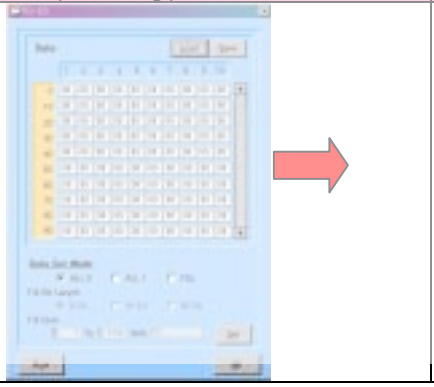
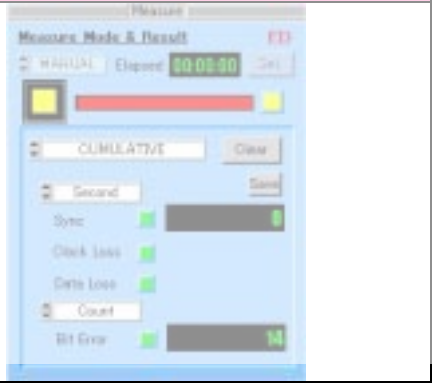
Example of a measurement screen

Basic screen



Example of transmitting pattern setting (SDH base)	Transmitting pattern (CID)	Example of receiving pattern setting (PRBS)
		

● Performance test using Program pattern

Set up transmitting pattern	Set up receiving pattern	Measurement result
		

Specifications

1. Clock source part of interface

Clock output	Frequency	10.6642GHz, 9.95328GHz, 2.66606GHz, 2.48832GHz
	Frequency Accuracy	± 4.6ppm
	Frequency Offset	± 50ppm （1ppm/step）
	Duty	50% ± 5%
	Output Level	1Vpp (Nominal value)
	Connector	APC-3.5
	Output Impedance	50Ω Ground terminal
External Synchronization Signal Input	Frequency	155.52MHz, 166.63MHz
	Frequency Tolerance Range	± 100ppm
	Input Level	More than 0.6Vpp
	Duty	50% (Nominal value)
	Connector	SMA
	Input Impedance	50Ω Ground terminal
Clock Trigger Output	Frequency	155.52MHz: When Clock Output is 9.95G, 2.48GHz 166.63MHz: When Clock Output is 10.66G, 2.66GHz
	Waveform	Sine wave
	Duty	50% ± 5%
	Output Level	0.7Vpp, 50Ω
	Connector	SMA
	Output Impedance	50Ω Ground terminal

2. PPG part of Interface

Line Clock Input	Frequency		10.6642GHz, 9.95328GHz, 2.66606GHz, 2.48832GHz
	Frequency Tolerance Range		± 100ppm
	Signal Level		0.7 ~ 1.5Vpp
	Connector		APC-3.5
	Input Impedance		50Ω Ground terminal
Line Clock Output	Frequency		The frequency inputted into LINE CLOCK
	Duty		50% ± 10%
	Output Level		VH = 0V ± 0.3V, VL = -1V ± 0.3V, Vpp > 0.6V
	TR/TF (20-80%)		Less than 30ps
	Connector		APC-3.5
	Output Impedance		50Ω Ground terminal
Clock Output	Frequency		The frequency inputted into LINE CLOCK
	Duty		50% ± 10%
	Phase Condition		CLOCK rise is the center of data. Tolerance ± 20ps or less
	Connector		APC-3.5
	Output Impedance		50Ω Ground terminal
	Output Control		ON/OFF function (When set OFF, signal level is Ground level)
Data Output	Pattern Transmission	BER Measurement	PRBS Pattern: 2^7-1, 2^{15}-1, 2^{23}-1, 2^{31}-1 Program pattern: Program length 8192 Byte (Program step 1 - 16 byte [1 byte step], 16 - 8192 bytes [16 byte step])

PPG part (continue)

Data Output	Pattern	SDH Frame	SOH program: STM-64 mode: 576 byte x 9 = 5184 byte
	Transmission	Pattern	STM-16 mode: 144 byte x 9 = 1296 byte
			Payload: Program 8bit PRBS: 2^{15}-1, 2^{23}-1, 2^{31}-1 Scramble: 2^{7}-1 Scramble ON/OFF Scramble range is whole range except line 1 in SOH.

SOH	Payload 8bit Program Pattern
Full Programming	

	CID Pattern	SOH Program: STM-64 mode: 576 byte x 1 = 576 byte STM-16 mode: 144 byte x 1 = 144 byte CID Length: STM-64 mode: 0 - 256 byte (1 byte step) STM-16 mode: 0 – 64 byte (1 byte step) Payload: Program: PRBS: 2^{7}-1, 2^{15}-1, 2^{23}-1, 2^{31}-1

SOH	CID (0/ 1)	PRBS

	Output Level	VH = 0V ± 0.2V, VL = -1V ± 0.2V
	TR/TF (20 - 80%)	Less than 45ps
	Eye Opening	More than 400mV
	Phase Condition	CLOCK raise is the center of data. Tolerance: less than ± 20ps
	Polarity	Positive/negative
	Connector	APC-3.5
	Output Control	ON/OFF function (When set OFF, signal level is Ground level)
Inverting Data Output (Option)	Output Level	VH = 0V ± 0.2V, VL = -1V ± 0.2V
	TR/TF (20 - 80%)	Less than 45ps
	Eye Opening	More than 400mV
	Phase Condition	CLOCK rise is the center of data. Tolerance ± 20ps or less
	Polarity	Positive/negative
	Connector	APC-3.5
	Output Impedance	50Ω Ground terminal
	Output Control	ON/OFF function (When set OFF, signal level is -1V)
Pattern Trigger Output	Trigger Cycle	Trigger period of output pattern
	Duty	LOW level is an equivalent for 128 bits of output data.
	Output Level	VH = 0 ± -0.1V, VL = -1 ± 0.1V
	Connector	SMA
	Output Impedance	50Ω Ground terminal
PPG Error Trigger	Duty	LOW level is an equivalent for 128 bits of output data.
	Output Level	VH = 0 ± -0.1V, VL = -1 ± 0.1V
	Connector	SMA
	Output Impedance	50Ω Ground terminal
Error Addition	Mode	Single: 1 bit error addition
		Rate: 10^{-3} ~ 10^{-12} (Setting rate: m x 10-n, m = 1.0 ~ 9.9 [0.1 step] n = 3 ~ 12 [1 step]

3. ED part of interface

Line Clock Input	Frequency		10.6642GHz, 9.95328GHz, 2.66606GHz, 2.48832GHz
	Frequency Tolerance Range		±100ppm
	Input Level		0.4 ~ 1.4Vpp or 0/-1V
	Input Phase Condition		CLOCK raise is the center of data.
	Phase Margin		More than ± 30deg
	Phase Adjust (Option)		Auto search, Manual adjust (10GHz band only) Adjust range: 1 cycle of 10.6642GHz or 9.95328GHz
	Connector		APC-3.5
	Input Impedance		50Ω Ground terminal
Data Input	Pattern Reception	BER Measurement	PRBS pattern: 2^7-1, 2^{15}-1, 2^{23}-1, 2^{31}-1 Program pattern: program length 8192 bytes (Program step: 1 ~ 16 byte [1 byte step], 16 ~ 8192 bytes [16 bytes step]
		SDH Frame Pattern	SOH program: STM-64 mode: 576 byte x 9 = 5184 byte STM-16 mode: 144 byte x 9 = 1296 byte Payload: Program 8bit PRBS: 2^{15}-1, 2^{23}-1, 2^{31}-1 Scramble: 2^7-1 Scramble ON/OFF Scramble range is whole range except line 1 in SOH.
			SOH: Full Programming / Payload 8bit Program Pattern
		CID Pattern	SOH Program: STM-64 mode: 576 byte x 1 = 576 byte STM-16 mode: 144 byte x 1 = 144 byte CID Length: STM-64 mode: 0 ~ 256 byte (1 byte step) STM-16 mode: 0 ~ 64 byte (1 byte step) Payload Program: PRBS: 2^7-1, 2^{15}-1, 2^{23}-1, 2^{31}-1
			SOH / CID (0 / 1) / PRBS
	Input Level		VH = 0V ± 0.2V, VL = -1V ± 0.2V
	Operation Signal Level		More than 400mV
	Input Phase Condition		CLOCK raise is the center of data.
	Phase Margin		More than ± 30deg
	Polarity		Positive/Negative
	Connector		APC-3.5
Clock Output	Frequency		Frequency inputed into LINE CLOCK
	Duty		50% ± 10%
	Output Level		VH = 0V ± 0.3V, VL = -1V ± 0.3V, Vpp > 0.6V
	TR/TF (20-80%)		Less than 30ps
	Connector		APC-3.5
	Output Impedance		50Ω Ground terminal
	Duty		50% ± 5%
	Connector		SMA
	Output Impedance		50Ω Ground terminal

ED part (continue)

Slave Trigger Output	Trigger Cycle	1/64(10G band) or 1/16(2.5G band) of ED input frequency
	Duty	50% ± 5%
	Output Level	VH = 0V ± 0.1V, VL = -1V ± 0.1V
	Connector	SMA
	Output Impedance	50Ω Ground terminal
Error Trigger	Error Trigger Output	Generate pulse when it detects error.
	Duty	Low level is equivalent for 128 bits of output data.
	Output Level	VH = 0V ± 0.1V, VL = -1V ± 0.1V
	Connector	SMA
	Output Impedance	50Ω Ground terminal
Detect Function	SYNC Detection	Pattern synchronize detection
	Loss of Clock	Detect when Clock is not imputed.
Measurement Function	Manual Measurement	From the measure start button is pushed to the stop button pushed.
	Single measurement	1 measurement which was set measurement time by the user
	Repeat measurement	Repeat measurement which was set measurement time by the user
	Measurement Time	1 ~ 999 seconds or 1 ~ 999 minutes or 1 ~ 999 hours
	Measurement Result	Cumulative, Measurement period

4. Common part

Environment	Operation Temperature Range	5 ~ 35 degrees
	Operation Humidity Range	20 ~ 80%
Dimension/ Weight	Dimension	Module: 90(W) x 262(H) x 355(D) mm (VXI C-size 3 slots width) VXI frame mounted: 152(W) x 388(D) x 548(D) mm
	Weight	Module: 6kg, VXI frame mounted: 17kg
Power Consumption	+24V	1.0A
	+12V	1.0A
	+5V	8.0A
	-2V	1.0A
	-5.2V	2.0A
	-12V	2.0A
	-24V	1.0A
VXI bus	Device Type	Message Based Servant
	VXIbus Backplane	P1 and P2 (VXI specification 1.3 conformity)
	Indication	Access, Fail, Err Clock source part: 11GHz, 10GHz, 1.7GHz, 2.5GHz ED part: Gate, Sig, Sync, Bit
Accessories	Instruction Manual: 1pc, AP9943 Software(CD-ROM): 1pc, Connection cable(U link): 1pc, 50Ω Terminator: 4pcs	

5. Option

Option 1: Phase adjust function
Option 2: Data bar (inverted signal) output
} Please refer detail in specification

Specifications are subject to change without notice.

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